IN THE CLAIMS:

1. (currently amended) A computer system comprising:

at least two processing sets, each processing set including a main memory; and

a bridge connecting the processing sets,

wherein at least a first processing set further includes a dirty memory having dirty indicators for indicating dirtied blocks of the main memory of the first processing set, and

wherein the bridge includes a direct memory access controller that is operable to respond to ~~a fault~~ an error state by controlling the copying of the dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

2. (original) The computer system of claim 1, wherein the direct memory access controller is operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

3. (original) The computer system of claim 1, wherein the dirty memory comprises control logic operable to search the dirty memory for dirty indicators indicative of dirtied blocks.

4. (original) The computer system of claim 3, wherein the control logic is operable to output references to the dirtied blocks of the main memory to be copied.

5. (original) The computer system of claim 4, wherein the control logic is operable to buffer references to the dirtied blocks of the main memory to be copied.

6. (original) The computer system of claim 4, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

7. (original) The computer system of claim 1, wherein a block of main memory is a page of main memory.

8. (original) The computer system of claim 1, wherein each dirty indicator comprises a single bit.

9. (original) The computer system of claim 1, wherein the direct memory access controller is operable to instigate a search of the dirty memory for dirty indicators indicative of dirtied blocks.

10. (original) The computer system of claim 1, wherein each processing set includes a dirty memory.

11. (original) The computer system of claim 1, wherein the processing sets are operable in lockstep, the computer system comprising logic operable to attempt to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.

12. (currently amended) A method for reintegrating the main memory of a computer system comprising:

at least two processing sets, each processing set including a main memory; and

a bridge connecting the processing sets,

the method comprising:

recording an indicator of a block of the main memory of a first processing set that has been dirtied in a dirty memory in the first processing set; and

a direct memory access controller in the bridge responding to ~~a fault~~ an error state by controlling the copying of dirtied blocks of the main memory of the first processing set indicated in the dirty memory of the first processing set to the main memory of another processing set.

13. (original) The method of claim 12, wherein the direct memory access controller searches the dirty memory for dirty indicators indicative of dirtied blocks.

14. (original) The method of claim 12, wherein dirty memory control logic searches the dirty memory for dirty indicators indicative of dirtied blocks.

15. (original) The method of claim 14, wherein the control logic outputs references to the dirtied blocks of the main memory to be copied.

16. (original) The method of claim 15, wherein the control logic buffers references to the dirtied blocks of the main memory to be copied.

17. (original) The method of claim 15, wherein the references to the dirtied blocks comprises addresses for the dirtied blocks.

18. (original) The method of claim 12, wherein a block of main memory is a page of main memory.

19. (original) The method of claim 12, wherein each dirty indicator comprises a single bit.

20. (original) The method of claim 12, wherein the direct memory access controller instigates a search of the dirty memory for dirty indicators indicative of dirtied blocks.

21. (original) The method of claim 12, wherein the processing sets are operable in lockstep, the method comprising attempting to reinstate an equivalent memory state in the main memory of each of the processor following a lockstep error.

22. (new) The computer system of claim 1, wherein the error state is due to a lockstep error, wherein said direct memory access controller controlling the copying of the dirtied blocks of the main memory of the first processing set to the main memory of another processing set is part of a reintegration process to reinstate an equivalent memory state in the main memory of each of the processing sets following the lockstep error.

23. (new) The computer system of claim 3, wherein each processing set further comprises a buffer, wherein the control logic is operable to store in the buffer addresses of the dirtied blocks of the main memory to be copied, wherein during a reintegration process the direct memory access controller is operable to access the buffer to determine whether any blocks of the main memory of the first processing set are dirtied.

24. (new) The computer system of claim 23, wherein the first processing set further comprises a counter that is operable to indicate a number of addresses corresponding to the dirtied blocks to be copied, wherein the number is incremented by the control logic each time an address is added to the buffer, and the number is decremented by the direct memory access controller each time the direct memory access controller copies a dirtied block of the main memory in the first processing set to the another processing set.

25. (new) The computer system of claim 23, wherein the buffer comprises a start pointer and an end pointer, wherein the start and end pointers encompass a portion of the buffer containing addresses of the dirtied blocks of the main memory to be copied.

26. (new) The computer system of claim 3, wherein the control logic is operable to directly provide the direct memory access controller addresses of the dirtied blocks of the main memory to be copied.

27. (new) The computer system of claim 2, wherein the direct memory access controller comprises a counter that is operable to count a number of dirtied blocks found in the main memory of the first processing set.

28. (new) The computer system of claim 3, wherein the dirty indicators being stored in groups with each group having associated therewith a parity indicator computed from the dirty indicator values of the group, wherein the control logic being operable on reading the dirty indicators of a group and a corresponding parity indicator to calculate a parity indicator value based on the dirty indicator values read for the group to determine an integrity of the group, wherein the control logic is configured to identify all dirty

indicators of the group as representing a dirtied state where the calculated parity indicator value is different from the parity indicator value read for that group.

29. (new) The computer system of claim 3, wherein the dirty memory comprising:

a lower level memory operable to store groups of dirty indicators, wherein each dirty indicator being associated with a respective block of main memory and being settable to a predetermined state to indicate that the block of main memory associated therewith has been dirtied;

at least one higher level memory operable to store groups of dirty group indicators, wherein each dirty group indicator being settable to a given state indicative that a group of dirty indicators of the lower level memory has at least one dirty indicator in the predetermined state indicative that a block of main memory associated therewith has been dirtied;

wherein the control logic is operable to read a dirty group indicator from the higher level memory and to treat the group of dirty indicators associated therewith as dirtied in response to the dirty group indicator having the given state; and

wherein, in response to the dirty group indicator having the given state, for each dirty indicator in the group of dirty indicators, the control logic is operable to read the dirty indicator from the lower level memory and to treat the block of main memory associated therewith as dirtied in response to the dirty indicator having the predetermined state.